ExTc / III / CBCGS 4/12/

Paper / Subject Code: 51203 / Digital System Design

(3 Hours) Max Marks: 80

1. Question No. 1 is compulsory.
2. Out of remaining questions, attempt any three questions.
3. Assume suitable additional data if required.
4. Figures in brackets on the right hand side indicate full marks.

(A) Explain Static RAM. (05)

(B) Compare Moore and Mealy machines. (05)

(C) Which of the following expression is equivalent to $Z = \overline{A(AB)}\ \overline{B(AB)}$ (10)

i) $Z = A \oplus B$ ii) $Z = \overline{A \oplus B}$

iii) $Z = A + B$ iv) $Z = AB$

Prove it.

(D) Perform the following operation using 2's compliment (05)

i) $(46)_{10} - (23)_{10}$

ii) $(23)_{10} - (46)_{10}$

Comment on results of (i) and (ii). (02)

(A) Compare Combinational circuits with Sequential circuits. (05)

(B) Convert the following into BCD and Octal code (05)

i) $(AB)_{16}$ ii) $(118)_{10}$

(C) Draw and explain a neat circuit diagram of BCD adder using IC 7483. (10)

(A) Minimize the following expression using Quine McClusky Technique (10)

$F(A,B,C,D) = \sum m(1,3,7,11,15) + d(0,2,5)$

(B) Implement the following function using single 8:1 Multiplexer. (10)

$f(A,B,C,D) = \sum m(2,3,5,7,8,9,12,13,14,15)$

(A) What is excitation table? Explain the excitation table of SR flip flop. (05)

(B) Convert SR flip flop to JK flip flop. (05)

(C) What is shift register? Explain working of Serial In Serial Out. Give its applications. (10)

(A) Simplify the following expression using Boolean algebra: (05)

$Y(A,B,C) = \sum m(0,1,2,3,4,5,6,7)$

(B) Represent the following Boolean expression by min/max terms (05)

$Y(A,B,C,D) = (A + B + C)(\overline{A} + C + \overline{D})$

(C) Design synchronous counter using D-type flip-flops for getting the following sequence: $0 \rightarrow 2 \rightarrow 4 \rightarrow 6 \rightarrow 0$. Take care of lockout condition. (10)

(A) Write VHDL code for 3:8 Decoder. (05)

(B) Compare FPGA and CPLD. (05)

(C) Design Full Adder circuit using PLA. (10)

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